REMARKS

Applicants acknowledge that the examiner indicated that claims 1-7, 27-29, 33-35, 43, and 45 are allowable, but have outstanding objections resulting from minor informalities. Applicants assume that claim 26 is also allowable subject to objections resulting from minor informalities. The examiner indicated that claims 39-41 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicants have amended claims 1-3, 6, 7, 26-28, 34, and 35 to correct minor informalities. Claim 37 has been amended to include the limitations of claims 38 and 39.

In addition, Applicants amended claims 1 and 26 to change the limitations "during a read phase" and "during a write phase" to "when pushing data to the processing agent," and "when pulling data from the processing agent," respectively. In claims 1, 6, 26, 34, 35, 37, and 41, the limitations "input transfer register" and "output transfer register" have been changed to "input transfer memory" and "output transfer memory," respectively.

Claim rejections

Claims 13, 16-19, 37, 38, 44, 49, 50, 52 and 53 were rejected under 35 U.S.C 103(a) as being unpatentable over Singhal in view of Misra.

Claims 20, 21, 51 and 54 were rejected under 35 U.S.C 103(a) as being unpatentable over Singhal and Misra, in view of Dennin.

Claims 13 and 16-21

Singhal and Misra do not disclose and would not have made obvious a push bus to push data from a plurality of memory resources to a processing agent, and a push bus arbiter to arbitrate use of the push bus by the memory resources, the memory resources obtaining access to the push bus based on arbitration by the push bus arbiter, wherein data are transferred unidirectionally on the push bus, as recited in amended claim 13.

Singhal discloses a computer system having plug-in circuit boards 50-N that each includes UPA CPU devices and on-board RAM (col. 6, lines 7-11). The CPU on each board can initiate read-type transactions to request transfer of data through a Data Bus from another board. Arbitration units 186 are used to arbitrate the use of the Data Bus by multiple circuit boards. In Singhal, the transfer of data on the Data Bus is not unidirectional. Data can be transferred from, e.g., circuit board 50-1 to circuit board 50-2, or from circuit board 50-2 to circuit board 50-1.

Misra discloses a processor local bus that includes a read data bus and a write data bus. Combining Singhal and Misra may have suggested a computer system having separate read and write data buses that are shared by multiple plug-in circuit boards. However, since each of the circuit boards can request data from another board, data would not be transferred unidirecitonally on the read data bus.

Claims 16-21, which depend directly or indirectly on claim 13, are allowable at least for the reasons discussed in claim 13. Moreover, these claims add additional distinctive features and are allowable in view of the cited references. For example, claim 16 recites "a plurality of context relative registers." Claim 21 recites "after the read command is processed, the memory controller is to push the data to an input transfer register of the processing agent and the processing agent is to read the data in the input transfer register and to continue the execution of the context." The cited references do not suggest at least these features of claims 16 and 21.

Claims 49-51

Singhal and Misra do not disclose and would not have made obvious using a push bus arbiter to arbitrate use of a push bus by a plurality of memory resources, data being transferred unidirectionally on the push bus, as recited in amended claim 49, for at least similar reasons as claim 13.

Claims 50 and 51, which depend directly or indirectly on claim 49, are allowable for at least the same reasons as claim 49. Moreover, these claims add additional distinctive features and are allowable in view of the cited references. For example, claim 50 recites executing a context and issuing a read command to a memory controller to read data from one of the memory

resources. Claim 51 recites swapping out the context if the data to be read is required to continue the execution of the context. The cited references do not suggest at least these features of claims 50 and 51.

Claims 52-54

Singhal and Misra do not disclose and would not have made obvious using a pull bus arbiter to arbitrate use of a pull bus by a plurality of memory resources, data being transferred on the pull bus unidirectionally, as recited in amended claim 52.

As discussed above, the combination of Singhal and Misra may have suggested a computer system having separate read and write data buses that are shared by multiple plug-in circuit boards. However, since each of the circuit boards can write data to another board, data would not be transferred unidirecitonally on the write data bus.

Claims 53 and 54, which depend directly or indirectly on claim 52, are allowable for at least the same reasons as claim 52. Moreover, these claims add additional distinctive features and are allowable in view of the cited references. For example, claim 53 recites executing a context and issuing a write command to a memory controller to write data to one of the memory resources. Claim 54 recites swapping out the context if completion of the write command is required to continue the execution of the context. The cited references do not suggest at least these features of claims 53 and 54.

New claim 55

Singhal and Misra do not disclose and would not have made obvious a push bus arbiter to arbitrate use of a unidirectional push bus by a plurality of memory resources, as recited in claim 55, for at least similar reasons as claim 13. Singhal and Misra do not disclose and would not have made obvious a pull bus arbiter to arbitrate use of a unidirectional pull bus by the memory resources, as recited in claim 55, for at least similar reasons as claim 52.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner. Any circumstance in which the applicant has made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims. Any circumstance in which the applicant has amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Enclosed is a $600 check for the excess claim fee and a $120 check for the petition for extension of time fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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